Applicant's response of July 11, 2003 pointed out that, to the contrary, Applicant's specification explicitly recites support for the clause, "without mass separation," and identified support for that claim term within the specification at, for example, page 11, lines 9-17; page 21, lines 1-12; and page 33, lines 10-17. Therefore, at that time, Applicant requested reconsideration and withdrawal of the rejection and of the Final Office Action.

Subsequently, due to circumstances explained fully in Applicant's Petitions of December 18, 2003 and July 20, 2004, the present application went abandoned, and was ultimately revived by virtue of the Decision on Petition of December 22, 2004. Upon the revival of the application, Applicant's undersigned representative contacted the Examiner to discuss the status of the present application.

As noted in the Interview Summary Form, the Examiner now takes the position that the claim limitation (emphasis in original): "introducing ions of a p-type impurity into at least a portion of only the first semiconductor island **without mass separation** wherein the portion is to become a channel region of a thin film transistor" also lacks support for the phrase "into at least a portion of only the first semiconductor island," as opposed to the second semiconductor island.

In response, Applicant respectfully submits, as also noted in the Interview Summary Form, that this position is not supported on the record. Specifically, Applicant submits that it is clear from a reading of the Final Office Action of March 13, 2003 (the pertinent language being quoted above) that the claim terms at issue were, "without mass separation." As such, Applicant requested a new Final Office Action in order to issue and explain the new grounds of rejection, which request was denied.

As a result, and in order to further prosecution of the application, Applicant respectfully requests continued examination of this application in light of the Request for Continued Examination (RCE) filed herewith. Further, regarding the present rejection of claims 1, 2, 6, 7, 12-16, 38, and 46 under 35 U.S.C. 112, first paragraph, based on the claim limitation, "introducing ion of a p-type impurity into at least a portion of only the first semiconductor island without mass separation wherein the portion is to become a channel region of a thin film

transistor," Applicant respectfully submits that the claim limitation is described and enabled in its entirety by Applicant's specification.

For example, page 11, lines 2-17, as well as to FIG. 2B, describe and illustrate that (with emphasis added): "... a resist mask 206 covering the island-like semiconductor layer 204 which becomes the active layer of the n-channel TFT is formed again. Then, B ions, which are impurity elements for imparting p-type conductivity are <u>added to the island-like layer 205 **alone**</u> ... (p)lasma doping can be mentioned as an alternative method for (B) ion implantation, but without using mass separation." That is, FIG. 2B clearly illustrates, as recited in, for example, claim 1, "introducing (e.g., B) ions of a p-type impurity into at least a portion of only said first semiconductor island (e.g., island 205)," and the specification states at page 11, lines 14-18 that such "introducing" may be performed by "plasma doping ... without mass separation."

As another example, Applicant's specification states at page 33, lines 3-17 describes an implementation illustrated in FIGS. 15A-15C in which B ions are implanted into only a semiconductor island 1505, as shown in FIG. 15B, and describes specifically that the ions are added to the island 1505 "alone" (at line 9), and that such implantation may be performed "...without using mass separation" (at lines 14-15).

Based on the above, Applicant respectfully submits that the new rejection under 35 U.S.C. 112, first paragraph, is improper, and should be withdrawn. Since no substantive rejection of claims 1, 2, 6, 7, 12-16, 38, and 46 (as well as claims 55-63, which Applicant believes to have been inadvertently withdrawn, as noted above) exists, Applicant respectfully submits that all of these claims should now be passed to allowance.

Regarding claims 64-68, Applicant submits that these claims also are in condition for allowance, based on the Applicant's comments included with Applicant's response of July 11, 2003, which are reproduced here for the Examiner's convenience.

Specifically, for example, claim 64 recites,

> forming a layer of a crystalline semiconductor film on a surface of a substrate, where the layer includes a portion to be used as a channel region of a thin film transistor;
> introducing ions of a p-type impurity into the portion;
> selecting a temperature corresponding to a mobility of the ions with respect to an interface between the crystalline semiconductor film and an oxide;
> subjecting the layer to a thermal oxidation process at the temperature to form a thermal oxide on the layer into which a portion of the ions diffuse from the crystalline semiconductor film, such that a desired concentration gradient of the ions within the crystalline semiconductor film is obtained that provides a corresponding adjustment to a threshold voltage of the thin film transistor.

Support for this claim is proved throughout the specification, including, for example, at page 12, line 6 to page 14, line 19. Specifically, as shown in FIGS. 4 and 5A, Boron has a diffusion coefficient that varies with temperature. Thus, by performing thermal oxidation at a particular temperature, the diffusion of (in this case) Boron may be finely controlled, so that an amount of Boron that diffuses out of a silicon layer and into an adjoining silicon oxide layer may be controlled. Thus, the Boron remaining in the silicon layer (i.e., in the channel region of a transistor) may be controlled so as to demonstrate a desired effect on the threshold voltage of the transistor.

In contrast, for example, Yamazaki '563 merely illustrates a doping/thermal oxidation process for a transistor (e.g., see FIG. 21C), in which some residual diffusion of previously-doped Boron may occur during a subsequent oxidation process. However, there is no disclosure or suggestion in Yamazaki '563 of "selecting a temperature corresponding to a mobility of the ions with respect to an interface between the crystalline semiconductor film and an oxide," as recited in new claim 64.

Moreover, there is no disclosure or suggestion in Yamazaki '563 of obtaining "a desired concentration gradient of the ions within the crystalline semiconductor film … that provides a

corresponding adjustment to a threshold voltage of the thin film transistor," as also recited in claim 64.

In this regard, it should be noted that Yamazaki does not appear to provide any teaching regarding an adjustment to a threshold voltage. For example, the August 14 Office Action points to the Abstract and column 21, lines 40-50 of Yamazaki '563 for this teaching. However, these sections deal only with a current leakage problem that results at sub-threshold levels.

That is, particular source/drain voltages imposed on a transistor may allow a drain current to flow even during a sub-threshold condition, as shown in FIG. 3. Yamazaki '563 proposes various solutions to this problem, including, for example, increasing a resistance within a channel region. In any case, modifying a threshold voltage of the transistor does not address this issue, and is not discussed in this context in Yamazaki.

Based on the above, Applicant respectfully submits that new claims 64-68 are allowable, so that all pending claims are in condition for allowance, and requests such action in the Examiner's next official communication.

Enclosed is a $790.00 check for the Request for Continued Examination (RCE) fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: February 8, 2005

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